PhD Thesis

Study and design of a digital baseband transceiver for wireless network-on-chip architectures

Keywords: Wireless network-on-chip, digital baseband transceiver, CDMA (Code Division Multiple Access) multicore architectures, VLSI and FPGA design

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The evolution of Silicon technologies and requirement in data rate for High Performance Computing (HPC), involve large number of computation resources and faster components (e.g. processor, memories) to support the application needs. Adding more execution resources in a single chip increases the need for efficient on-chip communication media and the introduction of new kinds of interconnects therefore becomes one of the major challenges for next MPSoC (Multiprocessor System-on-Chip). Today, manycore architectures are the standard and they imply impressive gain in the domains of HPC and servers but also in the area of embedded systems. Applications in all these categories are greedy for parallelism and number of cores will continue to increase. So, tackling the interconnect bottleneck in terms of energy consumption and data rate is a key concern.

In this context, the aim of the “BBC” (on-chip wireless Broadcast-Based parallel Computing) project funded by CominLabs is to evaluate the feasibility of using on-chip wireless link and also to define new associated computing paradigms. Using wireless communications easily enables broadcast capabilities for Wireless Networks on Chip (WiNoC) or on board (WiNoB) and new management techniques for memories and parallelism. So, these new paradigms will be defined and evaluated during this project. The key elements taken into account, concern the improvement of power consumption, the estimation of achievable data rates, the flexibility and the reconfigurability, the size reduction and the easiness of parallelism and memory hierarchy management.

Thanks to the use of wireless links associated with CDMA (Code Division Multiple Access) access techniques and new broadcast capabilities, limitations due to interconnect can be largely reduced. So, two complementary originalities studied in BBC are (i) the evaluation of the contribution of RF-radio link for intra-chip or inter-board interconnects and (ii) the definition of new opportunities for parallelism management and concurrent memory accesses. Furthermore, the objective of this project will be to study how this specific communication medium can be combined with some other possible solutions, such as classical electrical or optical NoCs which could provide interesting characteristics. In particular, optical and wireless communications can provide very attractive solutions but maybe not in the same context.

In the context of BBC, this thesis will address the challenge of studying and designing new low-power wireless digital baseband transceivers based on CDMA access.

The multilayer and hierarchical wireless NoC is summarized in Figure 1. The considered system is decomposed at the board level into multiple chips, each chip being itself decomposed into multiple tiles (for example a cluster of P processors). We therefore distinguish the following communication scenarios: The first one will be used for intra-chip communications (WiNoC) and the second one for inter-chip communications (WiNoB). For intra-chip communications, conventional CDMA transmissions will be studied and implemented. Moreover, impulse-radio modulation should be evaluated since the proximity of the antenna is expected to minimize the analog front-end. Considering impulse-radio communications as a conventional bus could allow to significantly simplify the complexity of the radio interface. Combined with CDMA access technique, this could lead to an efficient and very flexible WiNoC. The relationship between the data coding and the different propagation channels could also be used to alter and thus to improve the different link budgets according to the positions of the various access points.

We envisage to study different techniques and to fairly compare them in terms of data rate, latency, power consumption and silicon area cost. These performance evaluations will be conducted for the different scenarios and for different propagation environments and distances. We currently believe that impulse-radio (IR), i.e. ultra-wide-band radio, should be used for short range communications while narrow-band radio combined with access techniques like CDMA should be used for longer distances at the intra-chip and inter-chip levels. Comparison with other modulation schemes, such as for example complex OFDM modulations, will be necessary. For very short

distances, performance and cost comparisons with wired communications are also mandatory. For the access layer we mainly envisage the use of CDMA as a mean to share the medium between the different blocks, tiles or chip. CDMA will be compared with other access techniques such as TDMA or OFDMA.

At the link, MAC, and PHY layers, we therefore propose to answer the following two questions:

- What are the best modulation schemes for intra-chip and inter-chip wireless communications in terms of data rate, power consumption and bandwidth efficiency?
- What is the access technique to efficiently share the medium between tiles or chips, as well as to enable the new features that we intend to push in the project (broadcast, flexibility, low-power)?
- Should we use error correcting codes to trade-off transceiver linearity, silicon area and transmission power against power consumption and data rate?

The final aim of this thesis is to design and implement the digital baseband transceivers for the considered communication scenarios with low-power and small footprint constraints. Designs will be carefully validated by simulation and synthesis will provide performance and power consumption of the transceiver and gateway blocks. A 28nm FDSOI technology will be targeted for the experiments. As far as inter-chip is concerned, an FPGA prototype of the transceiver will be designed for the demonstrator developed in the BBC project.

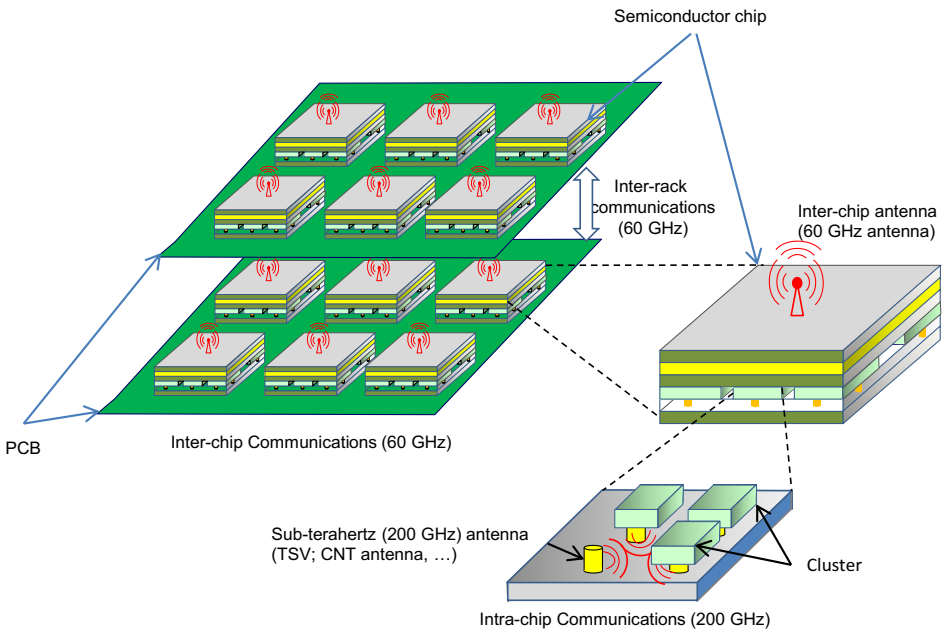

Figure 1: Wireless links and Network Hierarchy from Intra Cluster to Inter Chip

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