

Contributions of FPGA-based SDR in the context of vulnerabilities detection in the radio spectrum

Period: 36 months, from October 2016.

Fundings: Direction Générale de l'Armement (the French Government Defense procurement and technology agency).

Location: CentraleSupélec in IETR\SCEE research group (Rennes, France).

Advisors: Dr. Christophe Moy, Dr. Pascal Cotret.

Keywords: Partial reconfiguration, vulnerabilities detection, on-the-fly processing, signal detection, low-power systems, standard recognition.

PhD topics description

Recent progress in wireless communications pushed the proliferation of mobile communication systems (Internet of Things, connected devices, etc.). Nevertheless, such solutions created security breaches. Furthermore, software-defined radio architectures can be used to implement efficient auto-adaptative systems that may be hijacked in order to perform blind detection of unauthorized signals or even break their integrity (at the radio level).

In this study, we want to focus on the identification of vulnerabilities in the radio spectrum and to contribute, according to chosen waveforms, with efficient infiltration mechanisms. Current systems with similar goals are not efficient in terms of power consumption and physical size: target users must have one platform for each standard available in the spectrum.

The PhD student will study contributions in this field with software-defined radios and FPGA-based platforms: these reconfigurable architectures can be modified in real time. Such circuits can handle software radio algorithms and enable flexibility that may be accelerated thanks to Dynamic Partial Reconfiguration (DPR).

This project should contribute to the following areas:

- Efficient vulnerabilities detection in the radio spectrum with moderate costs in terms of power consumption and processing time.
- Resistance to software-defined radio (for instance, with a waveform implemented with difficulty in software radio).
- According to project progress, the PhD student could also take care of implementation security.

PhD context and requirements

The candidate will make his research at CentraleSupélec (Rennes campus) in the SCEE research group (http://www.supelec.fr/342_p_14858/telecommunications.html). The candidate will be co-supervised by Prof. Christophe Moy and Dr. Pascal Cotret. The candidate must have experiences with hardware design and signal processing knowledge. SCEE research group looks for an enthusiastic individual who is able to work independently, develop and discuss ideas. Knowledge of French language is not mandatory; however, good communication skills in English are necessary.

Application details

Application deadline: April 29th, 2016.

The applicant must hold a Master degree in digital electronics, computer science, signal processing or a related field. Please provide the following documents as a single ZIP archive to contacts provided below:

- Curriculum of the applicant.
- Detailed motivation letter with skills corresponding to the PhD thesis.
- If possible: grades and rankings of previous degrees, recommendation letter(s) from previous advisor(s) (with their complete name and coordinates as they may be contacted).

Contacts

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