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Thèse de doctorat

Titre : Accélération matérielle de la simulation de plateformes multi-coeurs hétérogènes

Title: Hardware Accelerated Simulation of Heterogeneous Multicore Platforms

Mots clés : architectures reconfigurables, FPGA, accélération matérielle, plateformes multi-coeurs hétérogènes, simulation, vérification
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Sujet/Subject

Heterogeneous multi-core architectures associating general-purpose processors, flexible network-on-chip and specialized accelerators (coarse-grain or fine-grain dynamically reconfigurable accelerators) provide the best trade-off between power, performance, cost and flexibility. When considering designing such hardware platforms, the number of possible design combinations leads to a huge design space, with subtle trade-offs and design interactions. To reason about what design is best for a given target application requires detailed simulation of many different possible solutions. Many software-based simulation frameworks have been developed, commercially and academically, but none of them really supports highly heterogeneous multi-core architectures (e.g. including Coarse Grain Reconfigurable Architectures). Moreover, they are generally designed around a single-threaded discrete-event simulation core [1] (e.g. SystemC, Simics, and Gem5-based platforms). As a consequence, the move to multi-core has hampered the performance of software-based simulators, since accurate multi-core simulation exposes complex non-deterministic behaviours. To tackle this simulation gap, several research groups have been working on hardware-accelerated architecture simulators. The most successful research has led to FPGA Accelerated Model Execution (FAME) techniques [2], where the desired target architecture is mapped to an FPGA for evaluation. Accelerated-FPGA simulators such as FAST [3], HAsim [4], Ramp Gold [5] and ProtoFlex [6] take advantage of these techniques. Indeed, modern FPGAs are perfect targets for implementing multi-core simulators. However, no existing framework targets highly heterogeneous architectures, even though both accurate and fast simulators are mandatory to design such machines.

This thesis is aimed at contributing to fill this hole by studying how highly heterogeneous multi-core architecture design can benefit from FPGA-accelerated simulation. Among many research challenges, the management of hardware accelerator (especially from an abstract simulation model point of view) and their accelerated simulation on FPGA will be at the heart of our concerns.

Références

[1] R. Leupers and O. Temam, Eds., Processor and System-on-Chip Simulation. Boston, MA: Springer US, 2010.
[2] Z. Tan, A. Waterman, H. Cook, S. Bird, K. Asanović, and D. Patterson, “A Case for FAME: FPGA Architecture Model Execution,” in Proceedings of the 37th Annual International Symposium on Computer Architecture, New York, NY, USA, 2010, pp. 290–301.
[3] D. Chiou, D. Sunwoo, J. Kim, N. A. Patil, W. Reinhart, D. E. Johnson, J. Keefe, and H. Angepat, “FPGA-Accelerated Simulation Technologies (FAST): Fast, Full-System, Cycle-Accurate Simulators,” in Proceedings of the 40th Annual IEEE/ACM International Symposium on Microarchitecture, Washington, DC, USA, 2007, pp. 249–261.
[4] M. Pellauer, M. Adler, M. Kinsy, A. Parashar, and J. Emer, “HAsim: FPGA-based high-detail multicore simulation using time-division multiplexing,” in 2011 IEEE 17th International Symposium on High Performance Computer Architecture (HPCA), 2011, pp. 406–417.
[5] Z. Tan, A. Waterman, R. Avizienis, Y. Lee, H. Cook, D. Patterson, and K. Asanović, “RAMP Gold: An FPGA-based Architecture Simulator for Multiprocessors,” in Proceedings of the 47th Design Automation Conference, New York, NY, USA, 2010, pp. 463–468.
[6] E. S. Chung, M. K. Papamichael, E. Nurvitadhi, J. C. Hoe, K. Mai, and B. Falsafi, “ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs,” ACM Trans. Reconfigurable Technol. Syst., vol. 2, no. 2, pp. 15:1–15:32, Jun. 2009.