Code optimizations for tight worst-case execution times (WCETs) on many-core architectures

Scientific context

Safety-critical systems (e.g. avionics, medical devices, automotive, ...) have so far used simple uni-core hardware systems in order to control their predictability, in order to meet timing constraints. Still, many critical embedded systems have increasing demand in computing power, and simple uni-core processors are not sufficient anymore. General-purpose multi-core processors are not suitable for safety-critical real-time systems, because they include complex micro-architectural elements (cache hierarchies, branch, stride and value predictors) meant to improve average-case performance, and for which worst-case performance (worst-case execution times, WCET) is difficult to predict.

Some architectures were designed with both performance and predictability in mind, and are good candidates to run critical real-time software. Examples of such architectures are the Kalray MPPA many-core architecture (http://www.kalrayinc.com) or the Recore many-core hardware (http://www.recoresystems.com/).

PhD proposal

The objective of this PhD thesis is to design code optimization methods enabling the calculation of tight worst-Case Execution Time (WCET) estimates on many-core architectures. The classes of considered code optimizations methods will emcompass:

- automatic code parallelization techniques, to automatically parallelize loop nests or applications developed in high-level models of computation
- code transformations and code generation techniques for tighter predictions of contentions to access shared resources (bus, network on chip, etc)
- code mapping techniques to optimize the end-to-end application execution time (e.g. mapping on the same core of communicating threads of the same aplication)
- local transformations of sequentiel codes enabling tight computations of WCETs, complementarily with existing work on the topic

The considered architecture will be a many core architecture a la Kalray/Recore. A side product of the PhD thesis could be the proposal of new architectural components for predictable many-cores.

Thesis supervisors will be members of the Alf and Cairn research groups (Alf for expertize on WCET computation, computer architecture and compilers, Cairn for automatic parallelization and compilers). The code optimization and WCET calculation techniques developed during the thesis will be integrated in the compiler and WCET calculation toolchains available in both groups.

Bibliographic references

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Keywords:

Real-time
Multi-core
Worst-case execution time estimation